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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/798,403	YOSHIOKA, SHINICHI	
	Examiner	Art Unit	
	LEON FLORES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims (1-20) have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Applicant asserts that, *"during a second test operation a first serializer converts parallel data into serial data synchronized with a clock generated by a first clock data recovery circuit. Further, during a first test operation a second serializer converts parallel data into serial data synchronized with a clock generated by a second clock data recovery circuit. As shown in the Attachment, the primary reference to Agrawal does not disclose or suggest the above-described structure".*

The examiner respectfully agrees. However, a new ground of rejection has been issued.

Applicant asserts that, *"in Goldrian the signal CLOCK_A in Figure 2, as an example, is generated based on the DATA_B transmitted from a driver module 211, and the signal CLOCK B is generated based on the DATA_A transmitted from a driver module 210 (see Goldrian at column 5, lines 30-45). In such ways Goldrian does not provide any disclosures that cure the deficiencies in Agrawal with respect to independent claim 20".*

The examiner respectfully agrees. However, a new ground of rejection has been issued.

Claim Objections

2. Claims (1-19) are objected to because of the following informalities:

In claims 1 & 12, the limitation of, *"in a normal operation and a first test operation"* is not explicitly taught in the specifications.

For the purpose of art considerations on the merits, this limitation will be construed as, when testing a particular receiver, transmitting serial data based on a transmit clock generated at the transmitter. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims (1-3, 6-7, 12, 14, 16-19) are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al (hereinafter Agrawal) (US Patent 7,098,685 B1) in view of Momtaz. (US Patent 7,099,278 B2)

Re claim 1, Agrawal discloses a semiconductor integrated circuit device comprising: a first receiver including a first clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated (See fig. 2: 202, RCVR + De-serializer CDR "with DPLL", col. 4, lines 42-44.); a second receiver including a second clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated. (See fig. 2: 206, RCVR + De-serializer CDR "with DPLL", col. 4, lines 42-44)

But the reference of Agrawal fails to explicitly teach a first transmitter including a first serializer which converts parallel data into serial data synchronized with one of a transmit clock in a normal operation and a first test operation, and a second transmitter including a second serializer which converts parallel data into serial data synchronized with one-of a transmit clock in a normal operation and the second test operation.

However, the reference of Agrawal does suggest the teachings of a first transmitter including a first serializer which converts parallel data into serial data synchronized with one of a transmit clock in a normal operation ("transmit based on a reference clock") and a first test operation ("the receiver and deserializer receives serial data & each receiver may operate in CDR mode") (See fig. 2: 202: TX + Serializer, col. 4, lines 31-44), and a second transmitter including a second serializer which converts parallel data into serial data synchronized with one-of a transmit clock in a normal operation ("transmit based on a reference clock") and the second test operation. ("the receiver and deserializer receives serial data & each receiver may operate in CDR

mode") (See fig. 2: 206: TX + Serializer, col. 4, lines 31-44)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Agrawal, in the manner as claimed, for the benefit of testing each SERDES.

The reference of Agrawal discloses the limitations as claimed above, except he fails to explicitly teach a first transmitter, which converts the parallel data into the serial data synchronized with the clock generated by the first clock data recovery circuit in a second test operation; and a second transmitter, which converts the parallel data into the serial data synchronized with the clock generated by the second clock data recovery circuit in the first test operation.

However, Montoz does. (See fig. 3 & col. 3, lines 29-64) Montoz discloses a system capable of operating in a normal mode and a loop back mode. The former transmit serial data using a reference clock and low speed clock. However, the latter transmit serial data using a clock generated by a clock data recovery circuit. The reference of Montoz further teaches that loop back testing is used to test the serial speed link between two locations. (See col. 1, lines 11-12) Furthermore, one skilled in the art would know that loop back testing is used to test transceivers.

Taking the combined teachings of Agrawal and Montoz as a whole, it would have been obvious to one of ordinary skills in the art to incorporate these features into the transceivers in the system of Agrawal, in the manner as claimed and as taught by Montoz, for the benefit of testing the serial high-speed link between two locations.

Re claim 2, the combination of Agrawal and Montoz further disclose that wherein the first and second transmitters are arranged between the first and second receivers, and the first and second transmitters are adjacent to the first and second receivers, respectively. (In Agrawal, see fig. 2. Furthermore, one skilled in the art would know that the element 204 can be placed either on top/bottom of both SERDERS "202 & 206" within the same chip. It is simply knowing how to route the wires when designing the PCB Board.)

Re claim 3, the combination of Agrawal and Montoz further disclose that wherein the first and second receivers are arranged between the first and second transmitters, and the first and second receivers are adjacent to the first and second transmitters, respectively. . (In Agrawal, see fig. 17. Furthermore, one skilled in the art would know that the element 204 can be placed either on top/bottom of both SERDERS "202 & 206" within the same chip. It is simply knowing how to route the wires when designing the PCB Board.)

Claim 6 has been analyzed and rejected w/r to claim 2 above.

Claim 7 has been analyzed and rejected w/r to claim 3 above.

Re claim 12, Agrawal discloses a semiconductor integrated circuit device comprising: a first receiver including a first clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a

phase of a clock to be generated on the basis of a frequency offset between the received serial data and a reference clock, or first phase control information for controlling a phase of a clock, and a first deserializer which converts serial data synchronized with the generated clock into parallel data (See fig. 2: 202, RCVR + De-serializer CDR "with DPLL", col. 4, lines 42-44. Furthermore, one skilled in the art would know that this is the way a CDR operates.); a second receiver including a second clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated on the basis of a frequency offset between the received serial data and a reference clock, or second phase control information for controlling a phase of a clock, and a second deserializer which converts serial data synchronized with the generated clock into parallel data. (See fig. 2: 206, RCVR + De-serializer CDR "with DPLL", col. 4, lines 42-44. Furthermore, one skilled in the art would know that this is the way a CDR operates.)

But the reference of Agrawal fails to explicitly teach a first transmitter including a first serializer which converts parallel data into serial data synchronized with one of a transmit clock in a normal operation and a first test operation, and a second transmitter including a second serializer which converts parallel data into serial data synchronized with one-of a transmit clock in a normal operation and the second test operation.

However, the reference of Agrawal does suggest the teachings of a first transmitter including a first serializer which converts parallel data into serial data synchronized with one of a transmit clock in a normal operation ("transmit based on a reference clock") and a first test operation ("the receiver and deserializer receives serial

data & each receiver may operate in CDR mode") (See fig. 2: 202: TX + Serializer, col. 4, lines 31-44), and a second transmitter including a second serializer which converts parallel data into serial data synchronized with one-of a transmit clock in a normal operation ("transmit based on a reference clock") and the second test operation. ("the receiver and deserializer receives serial data & each receiver may operate in CDR mode") (See fig. 2: 206: TX + Serializer, col. 4, lines 31-44)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Agrawal, in the manner as claimed, for the benefit of testing each SERDES.

The reference of Agrawal discloses the limitations as claimed above, except he fails to explicitly teach a first transmitter, which converts the parallel data into the serial data synchronized with the clock generated by the first clock data recovery circuit in a second test operation; and a second transmitter, which converts the parallel data into the serial data synchronized with the clock generated by the second clock data recovery circuit in the first test operation.

However, Momtoz does. (See fig. 3 & col. 3, lines 29-64) Momtoz discloses a system capable of operating in a normal mode and a loop back mode. The former transmit serial data using a reference clock and low speed clock. However, the latter transmit serial data using a clock generated by a clock data recovery circuit. The reference of Momtoz further teaches that loop back testing is used to test the serial speed link between two locations. (See col. 1, lines 11-12) Furthermore, one skilled in the art would know that loop back testing is used to test transceivers.

Taking the combined teachings of Agrawal and Momtoz as a whole, it would have been obvious to one of ordinary skills in the art to incorporate these features into the transceivers in the system of Agrawal, in the manner as claimed and as taught by Montoz, for the benefit of testing the serial high-speed link between two locations.

Re claim 14, the combination of Agrawal and Montoz fails to explicitly teach a test control pattern generator; and a test analyzer, wherein the test control pattern generator generates the first and second phase control information, and the test analyzer analyzes a state of the second clock data recovery circuit on the basis of the first phase control information and phase information of the clock recovered by the second clock data recovery circuit, and analyzes a state of the first clock data recovery circuit on the basis of the second phase control information and phase information of the clock recovered by the first clock data recovery circuit.

However, the reference of Agrawal does suggest a test control pattern generator (See fig. 2: REFCLK <0:3> from clock tree); and a test analyzer (See fig. 2: element 204 has a phase comparator. Furthermore, each receiver may employ its own DPLL), wherein the test control pattern generator generates the first and second phase control information (See fig. 2: the REFCLK is inputted to each SERDES), and the test analyzer analyzes a state of the second clock data recovery circuit on the basis of the first phase control information and phase information of the clock recovered by the second clock data recovery circuit, and analyzes a state of the first clock data recovery circuit on the basis of the second phase control information and phase information of the clock

recovered by the first clock data recovery circuit. (See fig. 2 & col. 4, lines 42-44. Each Receiver may employ its own PLL. Furthermore, one skilled in the art would know that each Receiver in elements 202 & 206 operate in the manner as claimed, providing each receiver is in CDR mode.)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Agrawal, as modified by Momtoz, in the manner as claimed, for the benefit of optimizing the communication system.

Claim 16 has been analyzed and rejected w/r to claim 2 above.

Claim 17 has been analyzed and rejected w/r to claim 3 above.

Claim 18 has been analyzed and rejected w/r to claim 2 above.

Claim 19 has been analyzed and rejected w/r to claim 3 above.

1. **Claims (4-5 & 8-11) are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al (hereinafter Agrawal) (US Patent 7,098,685 B1) and Momtaz. (US Patent 7,099,278 B2), as applied to claim 1, and further in view of Evans (US Publication 2003/0196139 A1).**

Re claim 4, the combination Agrawal and Momtaz fails to specifically disclose a first loop-back path which loops serial data from the first transmitter back to the second receiver; and a second loop-back path which loops serial data from the second transmitter back to the first receiver, wherein the first and second loop-back paths are formed in a semiconductor integrated circuit device chip.

However, Evans does. (See fig. 17B & paragraph 92) Evans discloses a first loop-back path which loops serial data from the first transmitter (0) back to the second receiver (1); and a second loop-back path which loops serial data from the second transmitter (1) back to the first receiver (0), wherein the first and second loop-back paths are formed in a semiconductor integrated circuit device chip. (See fig. 16B)

Taking the combined teachings of Agrawal, Momtaz and Evans as a whole, it would have been obvious to one of ordinary skill in the art to have incorporated this step into the system of Agrawal, as modified by Momtaz, in the manner as claimed and as taught by Evans, for the benefit of implementing automated self testing operations. (See paragraph 91)

Claim 5 has been analyzed and rejected w/r to claim 4 above.

Re claim 8, the combination of Agrawal, Momtaz and Evans further discloses a third loop-back path which loops serial data from the first transmitter back to the first receiver (See fig. 17A: element 0, and paragraph 92); and a fourth loop-back path which loops serial data from the second transmitter back to the second receiver (See fig. 17A: element 1, and paragraph 92), wherein the third and fourth loop-back paths are formed in the semiconductor integrated circuit device chip. (See fig. 16B)

Claim 9 has been analyzed and rejected w/r to claim 8 above.

Claim 10 has been analyzed and rejected w/r to claim 8 above.

Claim 11 has been analyzed and rejected w/r to claim 8 above.

6. Claims (13 & 15) are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al (hereinafter Agrawal) (US Patent 7,098,685 B1) and Momtaz. (US Patent 7,099,278 B2), as applied to claims 1 & 12 above, and further in view of Goldrian (US Patent 5,742,798).

Re claim 13, the combination of Agrawal and Momtoz fails to explicitly teach that wherein in the second test operation, the second receiver is to be tested, the first clock data recovery circuit changes a phase of a clock to be generated on the basis of the first phase control information, and outputs the phase-changed clock to the first transmitter, the first transmitter transmits, to the second clock data recovery circuit, serial data synchronized with the phase-changed clock output from the first clock data recovery circuit, and the second clock data recovery circuit receives the serial data transmitted from the first transmitter, and recovers the clock from the received serial data, and in the first test operation, the first receiver is tested, the second clock data recovery circuit changes a phase of a clock to be generated on the basis of the second phase control information, and outputs the phase-changed clock to the second transmitter, the second transmitter transmits, to the first clock data recovery circuit, serial data synchronized with the phase-changed clock output from the second clock data recovery circuit, and the first clock data recovery circuit receives the serial data transmitted from the second transmitter, and recovers the clock from the received serial data.

However, Goldrian does. (See figs. 2 & 6 & col. 3, lines 26-54 & col. 5, lines 13-

45). Goldrian discloses system for changing/adjusting the clocks of two chips based on the received data. Although the reference of Goldrian does not teach adjusting the clock signal based on CDRs, the concept of changing the clock based on the received data is taught and one of ordinary skills in the art would have founded obvious to use CDRs in order to adjust the clock signal. The reference of Goldrian further discloses that when the second receiver is to be tested (In Goldrian, when testing one of the chips), the first clock data recovery circuit changes a phase of a clock to be generated on the basis of the first phase control information (In Goldrian, see fig. 7B & col. 6, lines 27-56. Furthermore, Once the comparison has been made, if the comparison is not fulfilled delay A will be further incremented until chip A and B are synchronized.), and outputs the phase-changed clock to the first transmitter (In Goldrian, see col. 3, lines 48-54. There is a feedback line which connects the driver module to the variable clock delay.), the first transmitter transmits, to the second clock data recovery circuit, serial data synchronized with the phase-changed clock output from the first clock data recovery circuit (In Goldrian, see fig. 2 & col. 51-56), and the second clock data recovery circuit receives the serial data transmitted from the first transmitter, and recovers the clock from the received serial data (In Goldrian, Chip B receives the data. Furthermore, Goldrian teaches how two chips, having two different clocks, constantly communicating with each other, can achieve synchronization. But, Goldrian does not achieve synchronization by means of CDRs. However, Agrawal does. Thus, making this combination of references suitable for rejecting claim 13.), and when the first receiver is to be tested, the second clock data recovery circuit changes a phase of a

clock to be generated on the basis of the second phase control information, and outputs the phase-changed clock to the second transmitter, the second transmitter transmits, to the first clock data recovery circuit, serial data synchronized with the phase-changed clock output from the second clock data recovery circuit, and the first clock data recovery circuit receives the serial data transmitted from the second transmitter, and recovers the clock from the received serial data. (And vice versa, meaning, when testing the other chip.)

Taking the combined teachings of Agrawal, Momtoz and Goldrian as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system of Agrawal, as modified by Momtoz, in the manner as claimed and as taught by Goldrian, for the benefit of facilitating an optimization of the data transfer rate. (See col. 3, lines 25-26)

Re claim 15, the combination of Agrawal and Momtoz further discloses that wherein the test analyzer comprises a first test analyzing circuit which analyzes the state of the first clock data recovery circuit (In Agrawal, see fig. 2: the phase comparator in element 202), and a second test analyzing circuit which analyzes the state of the second clock data recovery circuit. (In Agrawal, see fig. 2: the phase comparator in element 206) the test control pattern generator comprises a first test control pattern generating circuit which generates the first phase control information (In Agrawal, see fig. 2: REFCLK <0:3> from clock tree).

But the combination of Agrawal and Momtoz fail to specifically disclose a second

test control pattern generating circuit which generates the second phase control information.

However, Goldrian does. (See fig. 5: 515 & col. 4, lines 48-51). Goldrian discloses a second test control pattern generating circuit which generates the second phase control information. Furthermore, each of the chips A & B contain a variable clock delay which adjusts the variable clock delay on each chip, allowing to synchronize chip clock A and B with respect to each other.

Taking the combined teachings of Agrawal, Momtaz and Goldrian as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system of Agrawal, as modified by Momtaz, in the manner as claimed and as taught by Goldrian, for the benefit of facilitating an optimization of the data transfer rate. (See col. 3, lines 25-26)

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al (hereinafter Agrawal) (US Patent 7,098,685 B1) in view of Goldrian (US Patent 5,742,798), and further in view of Wood, JR. (hereinafter Wood) (US Publication 2004/0228396 A1)

Re claim 20, Agrawal discloses a test method for a semiconductor integrated circuit device including a first receiver including a first clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated, a first transmitter including a first serializer which converts parallel data into serial data synchronized with one of a transmit clock

and the clock generated by the first clock data recovery circuit, a second receiver including a second clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated, and a second transmitter including a second serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock generated by the second clock data recovery circuit, the method comprising: when testing the first receiver, transmitting serial data synchronized with the phase-changed clock from the second transmitter to the first clock data recovery circuit (See fig. 2: 206: TX + Serializer, col. 4, lines 31-47); causing the first clock data recovery circuit to receive the serial data transmitted from the second transmitter, and to recover the clock from the received serial data. (See fig. 2: 202, RCVR + De-serializer CDR "with DPLL", col. 4, lines 42-44)

But the reference of Agrawal fails to explicitly teach analyzing a state of the first clock data recovery circuit on the basis of phase control information of the clock changed by the second clock data recovery circuit, and phase control information when the first clock data recovery circuit recovers the clock.

However, Goldrian does. (See figs. 2 & 6 & col. 3, lines 26-54 & col. 5, lines 13-45). Goldrian discloses system for changing/adjusting the clocks of two chips based on the received data. Although the reference of Goldrian does not teach adjusting the clock signal based on CDRs, the concept of changing the clock based on the received data is taught and one of ordinary skills in the art would have founded obvious to use CDRs in order to adjust the clock signal.

Taking the combined teachings of Agrawal and Goldrian as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system of Agrawal, in the manner as claimed and as taught by Goldrian, for the benefit of facilitating an optimization of the data transfer rate. (See col. 3, lines 25-26)

The combination of Agrawal and Goldrian discloses the limitations as claimed above, except they fail to teach causing the second clock data recovery circuit to change a phase of a clock to be generated regardless of serial data, and to output the phase-changed clock to the second transmitter.

However, Wood does. (See fig. 4B: 442, 446, 450 & paragraph 41) Wood suggests causing the second clock data recovery circuit (204b) to change a phase of a clock to be generated regardless of serial data (based on 450), and to output the phase-changed clock to the second transmitter.(446)

Taking the combined teachings of Agrawal, Goldrian, Wood as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system of Agrawal, as modified by Goldrian, in the manner as claimed and as taught by Wood, for the benefit of providing serial clocking to the transmit circuit. (See paragraph 41)

The combination of Agrawal, Goldrian, and Wood further discloses that when testing the second receiver, causing the first clock data recovery circuit to change a phase of a clock to be generated regardless of serial data, and to output the phase-changed clock to the first transmitter (In Wood, see fig. 4B: 442, 446, 450 & paragraph 41); transmitting serial data synchronized with the phase-changed clock from the first transmitter to the second clock data recovery circuit (In Agrawal, see fig. 2: 202: TX +

Serializer, col. 4, lines 31-47); causing the second clock data recovery circuit to receive the serial data transmitted from the first transmitter, and to recover the clock from the received serial data (In Agrawal, see fig. 2: 202, RCVR + De-serializer CDR "with DPLL", col. 4, lines 42-44); and analyzing a state of the second clock data recovery circuit on the basis of phase control information of the clock changed by the first clock data recovery circuit, and phase control information when the second clock data recovery circuit recovers the clock. (In Goldrian, see figs. 2 & 6 & col. 3, lines 26-54 & col. 5, lines 13-45)

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (hereinafter Chan) (US Publication 2003/0179771 A1) in view of Goldrian (US Patent 5,742,798), and further in view of Wood, JR. (hereinafter Wood) (US Publication 2004/0228396 A1)

Re claim 20, Chan discloses a test method for a semiconductor integrated circuit device including a first receiver including a first clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated, a first transmitter including a first serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock generated by the first clock data recovery circuit, a second receiver including a second clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated, and a second transmitter including a second serializer which converts parallel data into serial

data synchronized with one of a transmit clock and the clock generated by the second clock data recovery circuit, the method comprising: when testing the first receiver, transmitting serial data synchronized with the phase-changed clock from the second transmitter to the first clock data recovery circuit (See fig. 4: 424 to 410 via 434); causing the first clock data recovery circuit to receive the serial data transmitted from the second transmitter, and to recover the clock from the received serial data. (See fig. 4: 424 to 410 via 434)

But the reference of Chan fails to explicitly teach analyzing a state of the first clock data recovery circuit on the basis of phase control information of the clock changed by the second clock data recovery circuit, and phase control information when the first clock data recovery circuit recovers the clock.

However, Goldrian does. (See figs. 2 & 6 & col. 3, lines 26-54 & col. 5, lines 13-45). Goldrian discloses system for changing/adjusting the clocks of two chips based on the received data. Although the reference of Goldrian does not teach adjusting the clock signal based on CDRs, the concept of changing the clock based on the received data is taught and one of ordinary skills in the art would have founded obvious to use CDRs in order to adjust the clock signal.

Taking the combined teachings of Chan and Goldrian as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system of Chan, in the manner as claimed and as taught by Goldrian, for the benefit of facilitating an optimization of the data transfer rate. (See col. 3, lines 25-26)

The combination of Chan and Goldrian discloses the limitations as claimed

above, except they fail to teach causing the second clock data recovery circuit to change a phase of a clock to be generated regardless of serial data, and to output the phase-changed clock to the second transmitter.

However, Wood does. (See fig. 4B: 442, 446, 450 & paragraph 41) Wood suggests causing the second clock data recovery circuit (204b) to change a phase of a clock to be generated regardless of serial data (based on 450), and to output the phase-changed clock to the second transmitter.(446)

Taking the combined teachings of Chan, Goldrian, Wood as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system of Chan, as modified by Goldrian, in the manner as claimed and as taught by Wood, for the benefit of providing serial clocking to the transmit circuit. (See paragraph 41)

The combination of Chan, Goldrian, and Wood further discloses that when testing the second receiver, causing the first clock data recovery circuit to change a phase of a clock to be generated regardless of serial data, and to output the phase-changed clock to the first transmitter (In Wood, see fig. 4B: 442, 446, 450 & paragraph 41); transmitting serial data synchronized with the phase-changed clock from the first transmitter to the second clock data recovery circuit (In Chan, see fig. 4: 412 to 422 via 434); causing the second clock data recovery circuit to receive the serial data transmitted from the first transmitter, and to recover the clock from the received serial data (In Chan, see fig. 4: 412 to 422 via 434); and analyzing a state of the second clock data recovery circuit on the basis of phase control information of the clock changed by the first clock data recovery circuit, and phase control information when the second

clock data recovery circuit recovers the clock. (In Goldrian, see figs. 2 & 6 & col. 3, lines 26-54 & col. 5, lines 13-45)

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON FLORES whose telephone number is (571)270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/L. F./
Examiner, Art Unit 2611
September 29, 2008

/Kevin M. Burd/

Primary Examiner, Art Unit 2611